Application Number 09/994,508
Supplemental Amendment dated March 11, 2005

Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A method of fabricating a semiconductor device having a low dielectric interlayer insulation layer, the method comprising:

installing a semiconductor substrate in a chamber;

introducing a layer formation source gas into the chamber, the layer formation source gas being selected to provide atoms used in forming a silicon oxycarbide layer on the substrate, the layer formation source gas comprising at least one of: (i) at least one of N_2O and O_2 for supplying oxygen, (ii) a gas containing a methyl silane group selected from the group consisting of a gas containing a monomethyl silane group, a gas containing a dimethyl silane group, a gas containing a trimethyl silane group, and a gas containing tetramethyl silane, and (iii) another organic silicon gas;

introducing a first plasma source gas into the chamber;

performing plasma-enhanced chemical vapor deposition (PECVD) on the substrate in the chamber while the layer formation source gas and the first plasma source gas are being introduced into the chamber at a temperature of about 300 to 400 degrees C, the PECVD resulting in completely forming a silicon oxycarbide layer as the low dielectric interlayer insulation layer on the substrate;

~~stopping the introduction of the layer formation source gas into the chamber;~~

introducing a second plasma source gas into the chamber without the layer formation source gas at a temperature of about 250 to 400 degrees C, the second plasma source gas being at least one gas selected from the group consisting of He, H_2, N_2O, NH_3, N_2, O_2 and Ar;

using the second plasma source gas, treating the completely formed silicon oxycarbide

layer with plasma; and

stacking photoresist on the plasma-treated oxycarbide layer and patterning the resultant structure.

2. (Previously Presented) The method of Claim 1, wherein the the layer formation source gas comprises nitrogen atoms.

3. (Canceled)

4. (Previously Presented) The method of Claim 1, wherein forming the silicon oxycarbide layer and treating with plasma are performed in situ in the chamber.

5. (Original) The method of Claim 4, wherein forming the silicon oxycarbide layer and treating with plasma are performed under conditions of a pressure of 1 to 10 Torr and a temperature of 300 to 400°C.

6. (Original) The method of Claim 1, wherein forming the silicon oxycarbide layer and treating with plasma are performed under conditions of a pressure of 1 to 10 Torr and a temperature of 300 to 400°C.

7. (Canceled)

8. (Original) The method of Claim 1, wherein the photoresist is a chemical amplification type photoresist which generates hydrogen ions (H+) in a case of light exposure.

9. (Original) The method of Claim 8, wherein the patterning comprises:
exposing the photoresist to light below a photo mask;
performing a post exposure bake; and

developing the photoresist.

10. (Original) The method of Claim 1, wherein the patterning comprises:
exposing the photoresist to light below a photo mask;
performing a post exposure bake; and
developing the photoresist.

11. (Currently Amended) A method of fabricating a semiconductor device having a low dielectric interlayer insulation layer, comprising:

installing a semiconductor substrate in a chamber;

introducing a layer formation source gas into the chamber, the layer formation source gas being selected to provide atoms used in forming a silicon oxycarbide layer on the substrate, the layer formation source gas comprising at least one of: (i) at least one of N_2O and O_2 for supplying oxygen, (ii) a gas containing a methyl silane group selected from the group consisting of a gas containing a monomethyl silane group, a gas containing a dimethyl silane group, a gas containing a trimethyl silane group, and a gas containing tetramethyl silane, and (iii) another organic silicon gas;

introducing a first plasma source gas into the chamber;

performing plasma-enhanced chemical vapor deposition (PECVD) on the substrate in the chamber while the layer formation source gas and the first plasma source gas are being introduced into the chamber at a temperature of about 300 to 400 degrees C, the PECVD resulting in stacking a completely formed silicon oxycarbide layer (SiOC) as the low dielectric interlayer insulation layer on the substrate;

~~stopping the introduction of the layer formation source gas into the chamber;~~

introducing a second plasma source gas into the chamber without the layer formation source gas at a temperature of about 250 to 400 degrees C, the second plasma source gas being at least one gas selected from the group consisting of He, H_2, N_2O, NH_3, N_2, O_2 and Ar;

using the second plasma source gas, treating the completely formed silicon oxycarbide

layer with plasma; and

forming an interconnection at the silicon oxycarbide layer using a damascene process.

12. (Previously Presented) The method of Claim 11, wherein H_2-plasma is used as the second plasma source gas, and further comprising forming an insulation layer for capping on the silicon oxycarbide layer after treating with plasma and before forming the interconnection.

13. (Previously Presented) The method of Claim 12, wherein the layer formation source gas comprises at least one of a silane gas and a tetraethylorthosilicate (TEOS) gas.

14. (Previously Presented) The method of Claim 12, wherein treating with the second plasma source gas is performed under a H_2-ambient at a temperature of 250 to 400oC and a pressure of 1 to 10 Torr and by applying a radio frequency electric field.

15. (Currently Amended) The method of Claim 12, wherein forming the interconnection using the damascene process comprises:

forming a photoresist pattern over the silicon oxycarbide layer;

forming a groove at the top of the silicon oxycarbide layer using the photoresist pattern as an etch mask;

removing the photoresist pattern by an ashing method using O_2-plasma ~~at the groove-formed substrate~~;

sequentially stacking a barrier metal and a metal layer for interconnection at the groove-formed substrate to fill the groove; and

removing the metal layer for interconnection stacked at the top surface of the silicon oxycarbide layer using a chemical mechanical polishing (CMP) process.

16. (Original) The method of Claim 15, wherein the metal layer for interconnection is formed of copper.

17. (Original) The method of Claim 12, wherein the damascene process comprises forming the groove and then forming a contact hole at a region of the groove.

18. (Canceled)

19. (Original) The method of Claim 11, further comprising forming an organic polymer layer at the silicon oxycarbide layer using a coating method after treating with plasma and before forming the interconnection.

20. (Canceled)

21. (Original) The method of Claim 19, wherein forming the organic polymer layer is performed by a coating method at the substrate and then curing is performed at a high temperature of 400 to 450°C.

22. (Original) The method of Claim 19, wherein the damascene process is performed by a dual damascene method comprising forming a groove at the organic polymer layer using a patterning process and forming a contact hole at the silicon oxycarbide layer at a region of the groove through a patterning process.

23. (Canceled)

24. (Canceled)